What is claimed is:

1. A process for integrating an alignment mark and a trench device, comprising the steps of:

providing a substrate having a device region and an alignment mark region;

forming a first trench in the device region and a second trench in the alignment mark region, wherein the second trench has a width larger than the first trench;

forming a trench capacitor in each of the low portion of the first and second trenches;

forming a first polysilicon layer on the trench capacitor in each of the first and second trenches;

forming a second polysilicon layer overlying the substrate and filling in the first trench and simultaneously and conformably forming the second polysilicon layer over the inner surface of the second trench; and

removing the second polysilicon layer and a portion of the first polysilicon layer on the alignment mark region and simultaneously leaving a portion of the second polysilicon layer in the first trench on the device region by an etch back process.

2. The process as claimed in claim 1, wherein the substrate is a silicon wafer and the alignment mark region is at the scribe line of the wafer.

3. The process as claimed in claim 1, wherein the trench capacitor comprises:

a bottom electrode formed in the substrate around each of the lower portions of the first and second trenches;

a top electrode disposed in each of the lower portion of the first and second trenches; and

a capacitor dielectric layer disposed between the bottom and top electrodes.

4. The process as claimed in claim 1, wherein the first polysilicon layer has a thickness of about 2000Å to 4000Å.

5. The process as claimed in claim 1, wherein the second polysilicon layer has a thickness of about 2000Å to 4000Å.

6. The process as claimed in claim 1, wherein the etch back process comprises a polishing treatment to remove the second polysilicon layer overlying the substrate.

7. The process as claimed in claim 6, wherein the polishing treatment is chemical mechanical polishing.

8. A process for integrating an alignment mark and a trench device, comprising the steps of:

providing a substrate having a first trench and a second trench, wherein the second trench serves as the alignment mark and has a width larger than the first trench;

forming the trench device in each of the low portions of the first and second trenches;

forming a first conductive layer on the trench device in each of the first and second trenches;

forming a second conductive layer overlying the substrate and filling in the first trench and simultaneously and conformably forming the second conductive layer over the inner surface of the second trench; and

removing the second conductive layer and a portion of the first conductive layer in the second trench and simultaneously leaving a portion of the second conductive layer in the first trench by an etch back process.

9. The process as claimed in claim 8, wherein the substrate is a silicon substrate.

10. The process as claimed in claim 8, wherein the trench device is a trench capacitor.

11. The process as claimed in claim 10, wherein the trench capacitor comprises:

a bottom electrode formed in the substrate around each of the lower portion of the first and second trenches;

a top electrode disposed in each of the lower portions of the first and second trenches; and

a capacitor dielectric layer disposed between the top and bottom electrodes.

12. The process as claimed in claim 8, wherein the first conductive layer is a polysilicon layer.

13. The process as claimed in claim 12, wherein the first conductive layer has a thickness of about 2000Å to 4000Å.

14. The process as claimed in claim 8, wherein the second conductive layer is a polysilicon layer.

15. The process as claimed in claim 8, wherein the second conductive layer has a thickness of about 2000Å to 4000Å.

16. The process as claimed in claim 8, wherein the etch back process comprises a polishing treatment to remove the second conductive layer overlying the substrate.

17. The process as claimed in claim 16, wherein the polishing treatment is chemical mechanical polishing.